ABSTRACT OF THE DISCLOSURE

A backup memory, a DMA (direct memory access) controller, and a WDT (watch dog timer) are provided in addition to a CPU (central processing unit), a RAM (random access memory), and a peripheral circuit. The DMA controller exercises control so that respective data of the CPU, RAM and peripheral circuit is saved in the backup memory each time the CPU, being under normal operation, supplies a counter reset signal to the WDT, and so that the data that has been saved in the backup memory is restored to the CPU, the RAM and the peripheral circuit, respectively, if the WDT has detected a program runaway and outputted a time-over signal. Therefore, even in a case where a program runaway has occurred in the CPU, normal operation is permitted to be resumed from midway in the program.